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SUN Magnetics
INTEGRATED CIRCUIT INDUCTANCE EXTRACTION

INFRASTRUCTURE
Indaba
Engineering the Future now!

Technology and engineering innovation: software and start-ups

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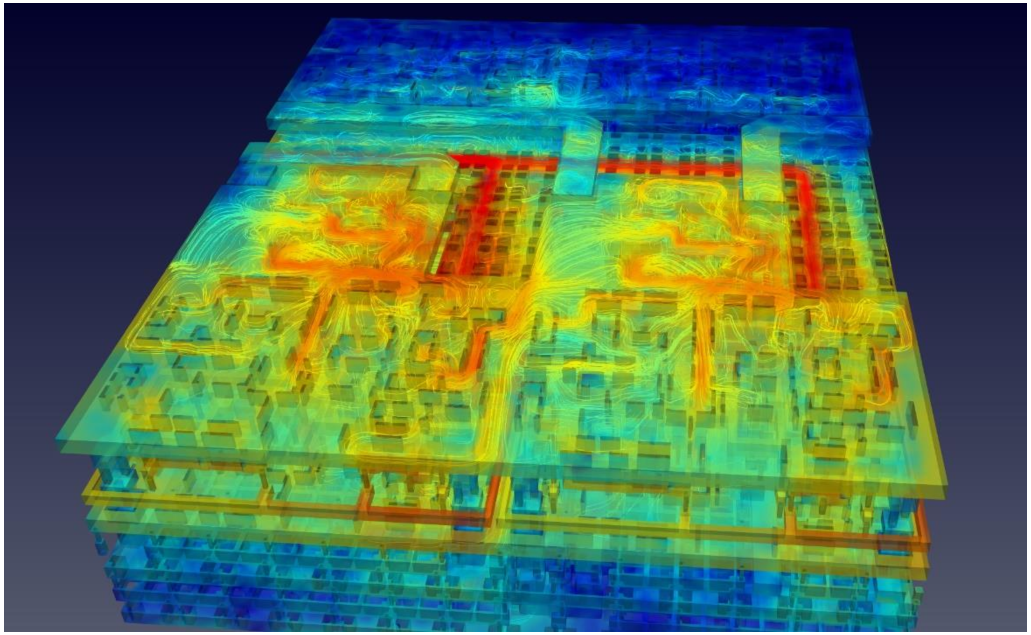
CEO SUN MAGNETICS

Introduction

Academia and innovation.

Academic spin-off companies and changing landscape.

Example: tools for design of quantum electronic circuits.



Academia and innovation

Academia still trains engineers.

Need to prepare engineering students for careers in an age where the pace of technological innovation is frenetic

The new engineer is no longer groomed for a lifetime career at a large parastatal or private company…

Today, the new engineer is forced by circumstance and technological evolution to innovate and take risk before their technological skill sets age.

- Start-ups and disruptive products and services.
- Postgraduate programmes develop these skills.

Pressure on academia

Government subsidies are plummeting.

Established industrial investment in student development (bursaries) are in decline.

New industries (especially in high technology) seldom invest in tertiary education.

How then to fund research programmes and development of engineers at postgraduate level?

- Grants, research contracts, innovation & spin-offs.

High cost of technology infrastructure

Consider electronics (**specifically integrated circuits**).

- The message is similar across technologies / engineering disciplines.

Up-front cost of laboratories, processes, plants for cutting edge engineering technology keeps rising.

- Semiconductor fabrication plant (fab):
  - 1990’s: ~US$1B
  - 2000’s: ~US$2-3B
  - 2010’s: ~US$5-10B
  - 2020: ~US$20-25B

Universities cannot afford cutting edge technology hardware / plants / R&D labs.

Government subsidies by some countries, and commercial pressure, have coalesced high-tech in very expensive fab nodes; typically in Far East.

- Not even local industry can afford such capital investment.

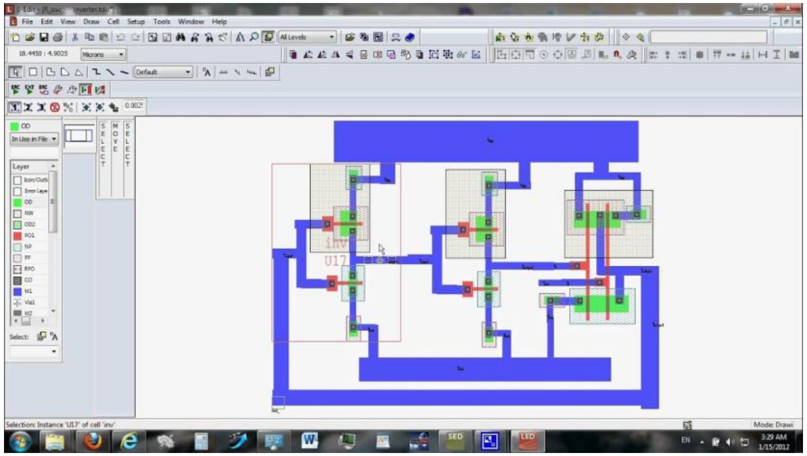
Innovation in academia

Out of necessity, industrial innovation in many advanced nations turned to “fabless” design of IP.

- Still expensive to fab and deliver electronics.

Locally, innovation focused on low cost of entry:

- Services that leverage electronics and computing resources – largely software-based.
- Design tools (software) that enable “fabless” design.



Academic perspective: advantages of algorithm/software development

Algorithm/software development fits very well with academic objectives:

- New engineers often pre-equipped with latest software development skills.
- Education develops skills and focuses these on engineering problems.
- No large capital expenditure or up-front costs involved.

Academic perspective: advantages of algorithm/software development

- “Retooling” when industrial application changes is often a light exercise.
- Development of engineers with light investment.
- Engineering algorithms form backbone of 4IR
  - Machine learning, AI, neural nets, cloud-based applications and services.
  - Uses computing technology without the need to actively develop computers.

Shifting landscape of spin-offs

Earlier Stellenbosch University spin-offs more hardware-oriented:

- Ocean-going vessels.
- Satellites.
- Medical devices.

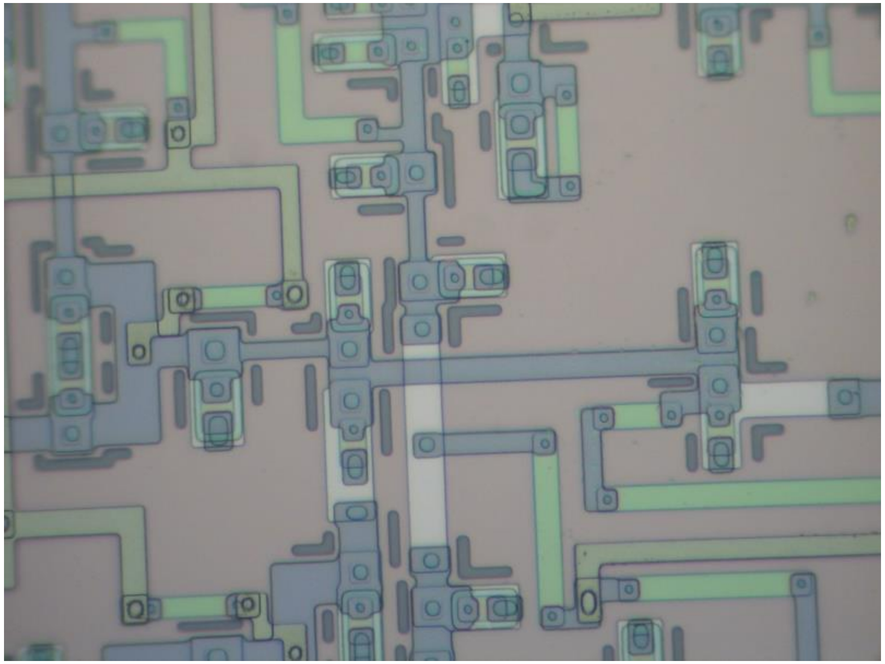
Recent SU spin-offs more software/IT service and IoT-oriented:

- Digital rights management / anti-piracy.
- Digital elevation maps / GIS.
- Electronic Design Automation software for quantum & superconductor electronics.

My perspective – superconducting quantum electronics

Clock speed up to max 300 GHz.

Low energy - ~1 000 times to 10 000 times less than CMOS per bit-switch (but need to be cooled to 4 K or less).



The economy of SCE

Data centres consume vast amounts of power – predicted to burn 20% of global energy by 2025.

Cryptocurrency energy use rising – more energy than some advanced countries.

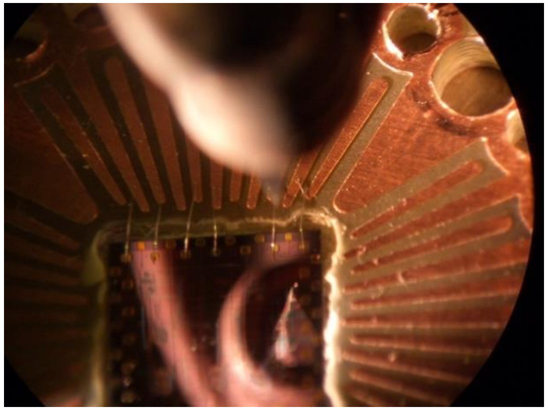
Energy-efficiency is key to new computing technologies – hence SCE.

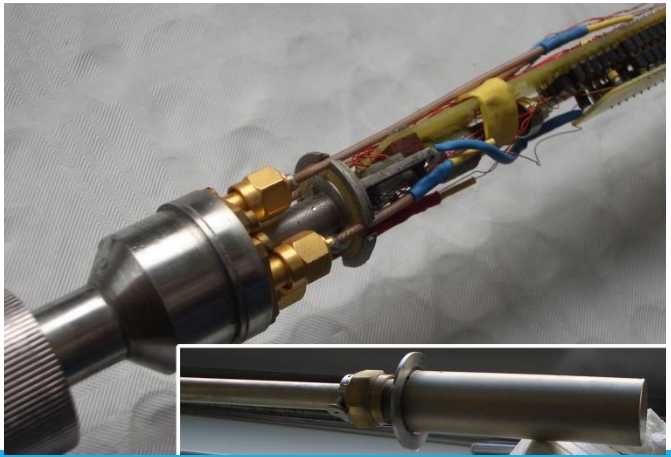
SCE used to implement certain flavours of quantum computer (enable flux qubits) – could open up vast computing applications and markets.

We have innovated on field-programmable SCE circuits, but hardware development cost is beyond SA capability.

Cryogenic equipment

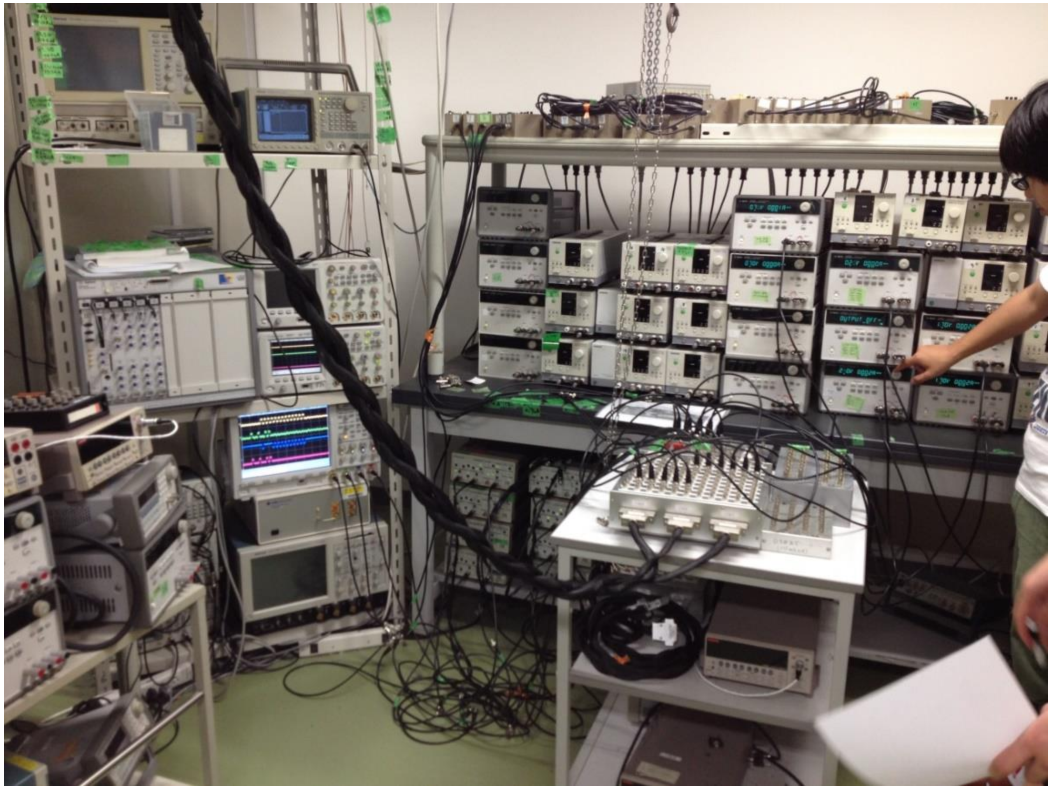
Magnetic fields, bias current, LiHe, 4 Kelvin (-269 °C) operation.





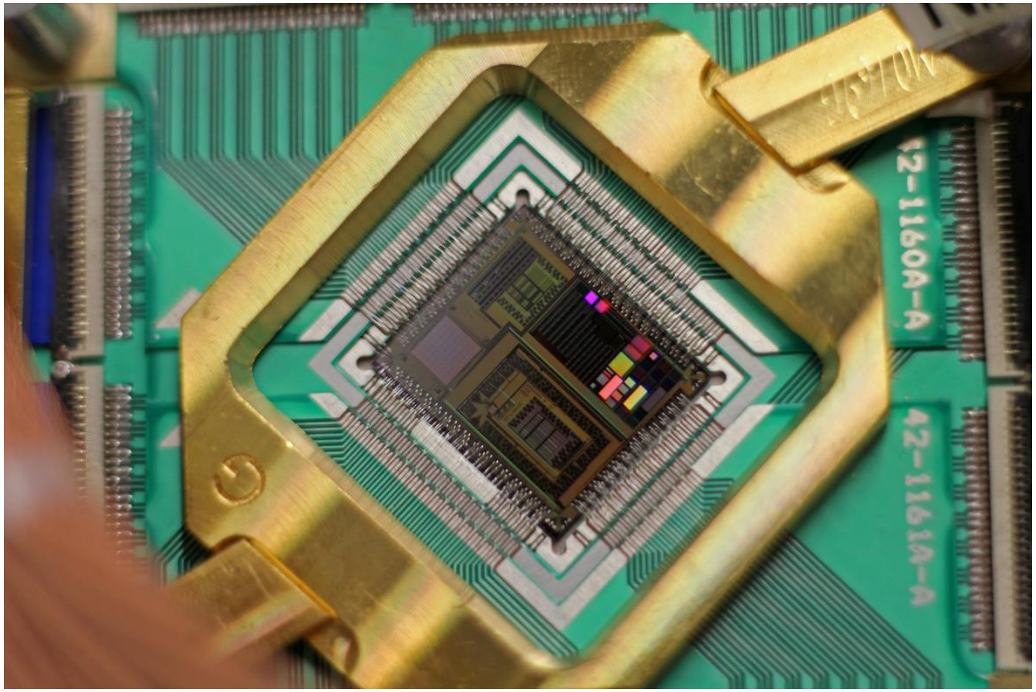
Test equipment

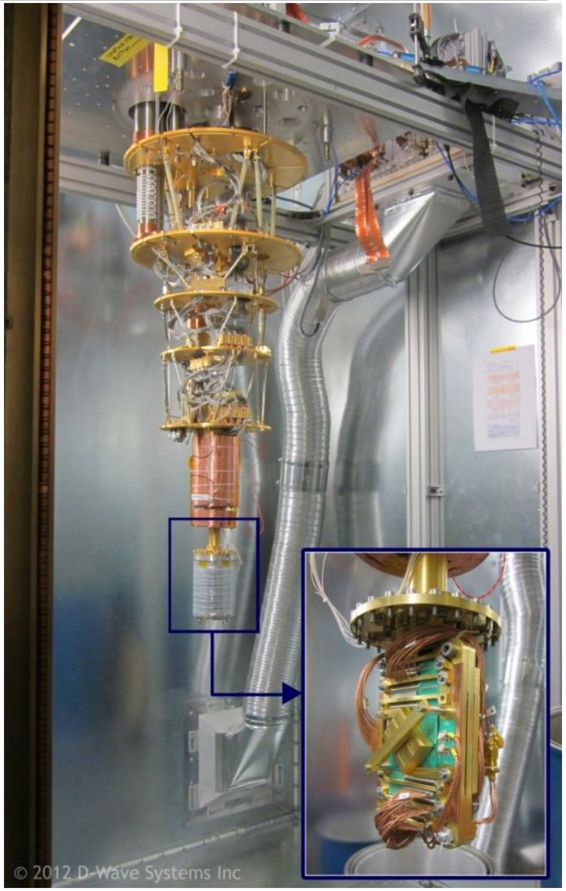
Expensive!



Magnetic shielding

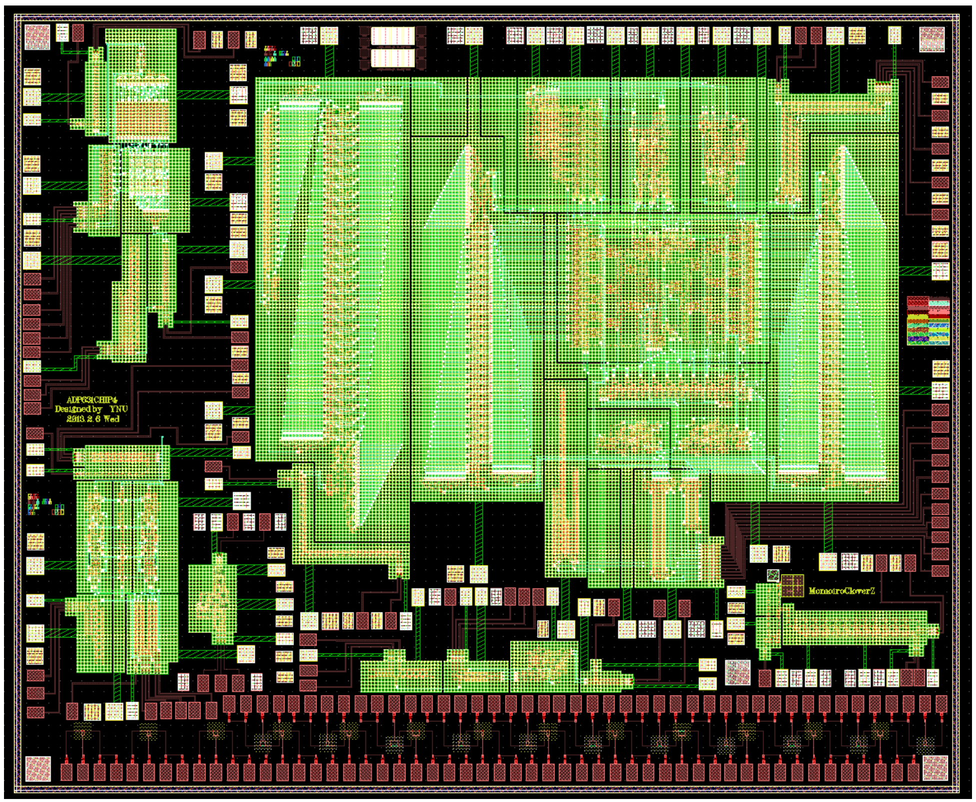
Cryocooler

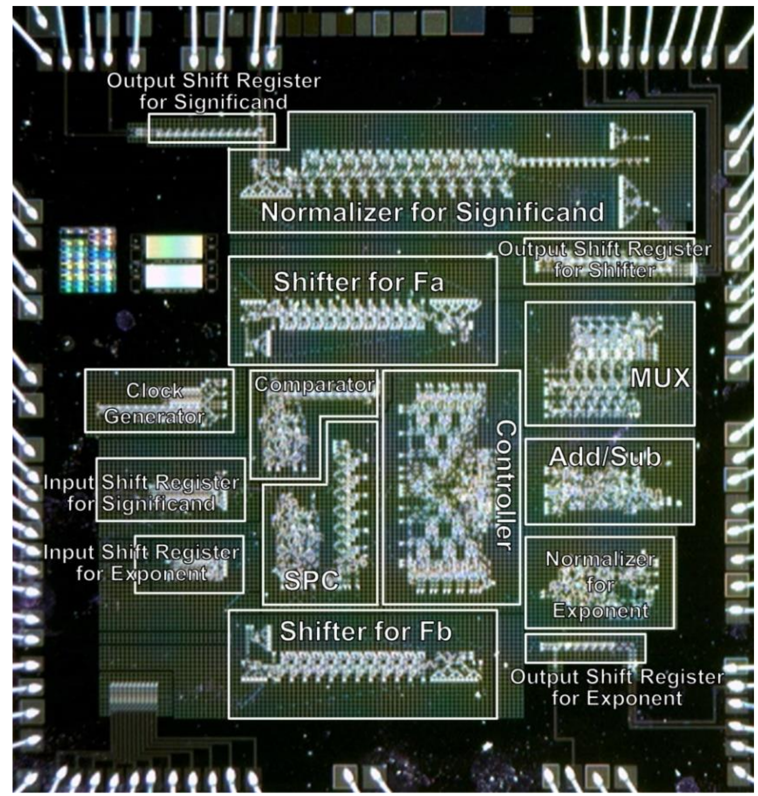




SFQ chip design

How to design this? If there are millions of components?



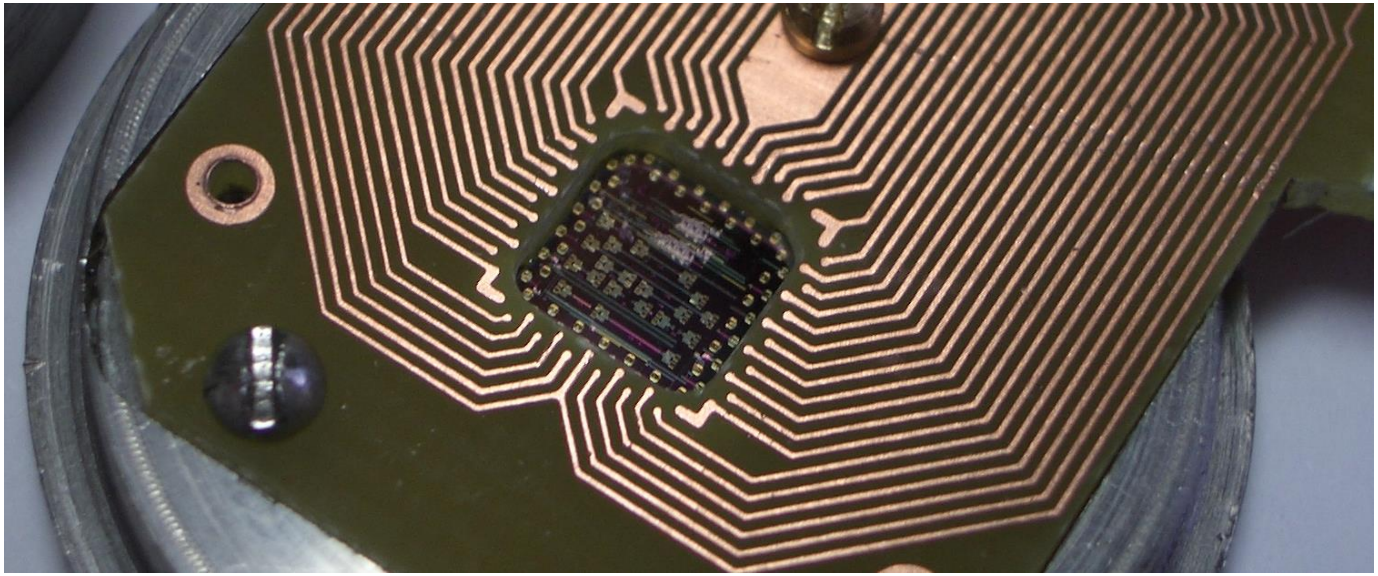


Cost of chip manufacture

Fab cost very high; wafer count very low on SCE/quantum.

- Consequently, a single chip is very expensive.

Turnaround time very long – 3-18 months.



EDA tools

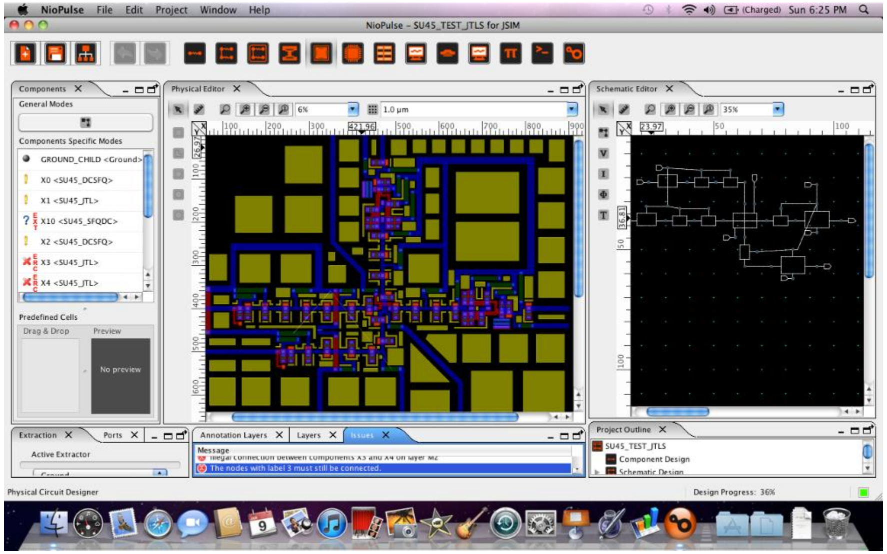
SU group identified low cost-of-entry R&D opportunity:

- No proper SCE design tools.
- We could not afford semiconductor Synopsys/Cadence, but these also not capable of designing SFQ circuits.
- Leading international groups use armies of students/researchers.
- We decided to build such tools for SFQ.
  - Did some exploratory software development from 2001 – 2004.

Commercial funding

2005: Pitched SCE EDA software idea for funding.

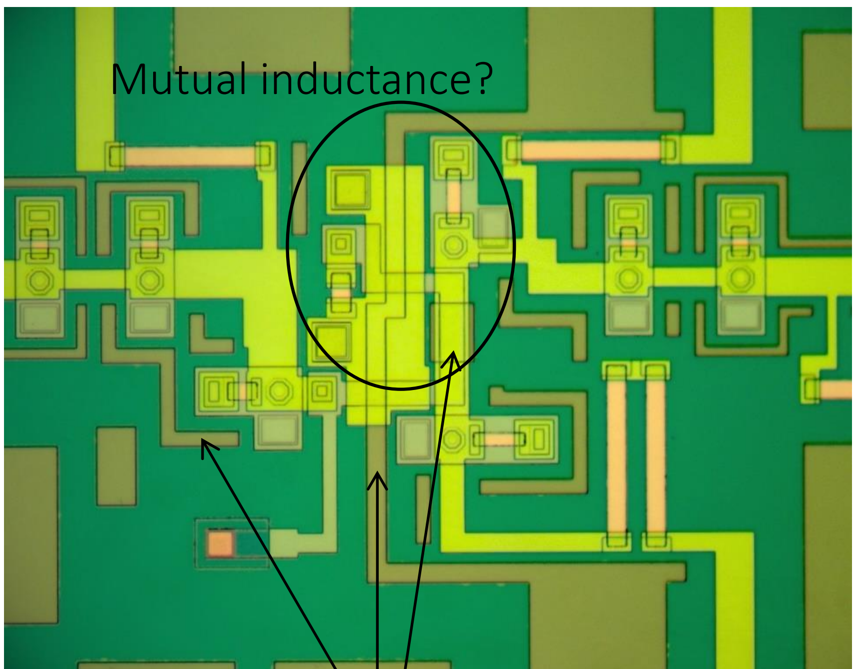
- "NioCAD" funded by NRF Innovation fund from 2007-2009.
- IDC investment from 2009 – 2012.
- Too early; market not developed, electronics and applications not mature – could not sell.
- Initial revenue model "up-front" cost and then yearly renewal fee – needed continuous growth.
- Team too large:
  Ran out of cash in 2012.

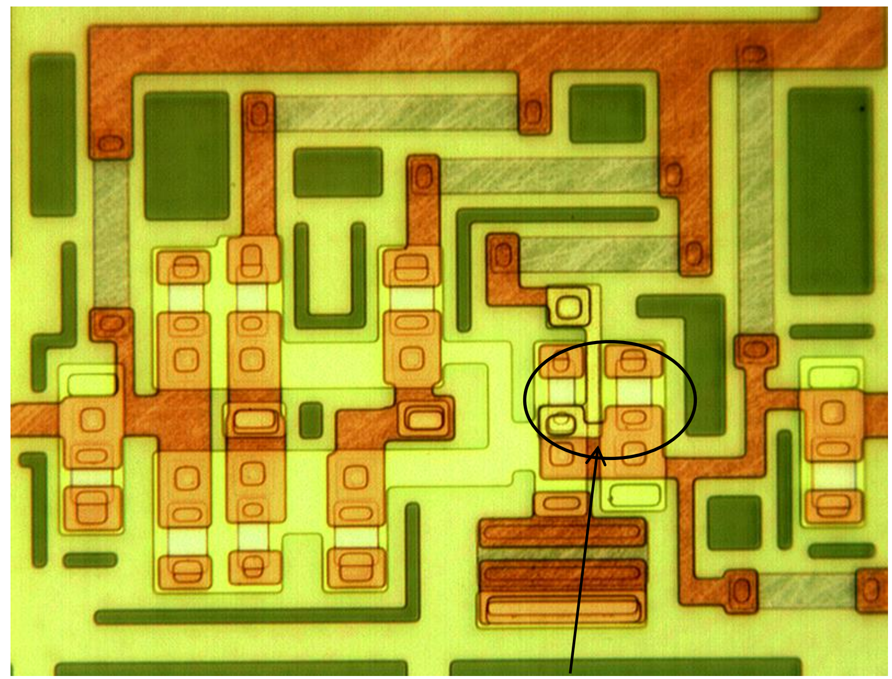


Self-funded: Inductance calculation in superconducting circuits

SFQ circuit operation very sensitive to inductance.

- Hard to calculate, but critical design parameter.

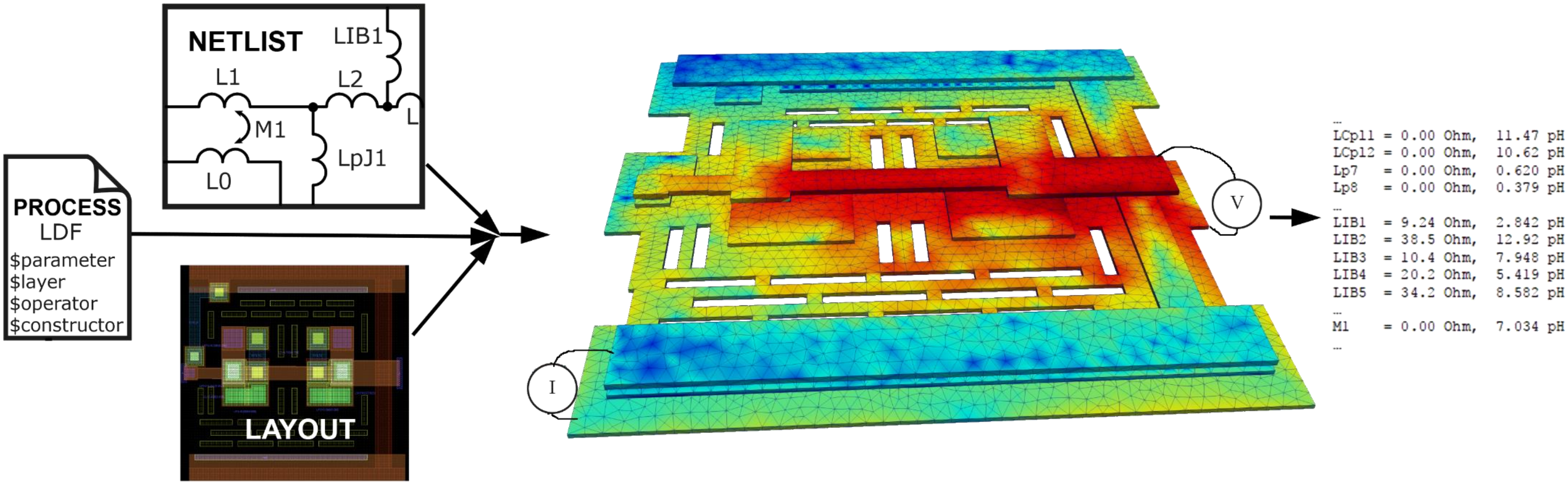




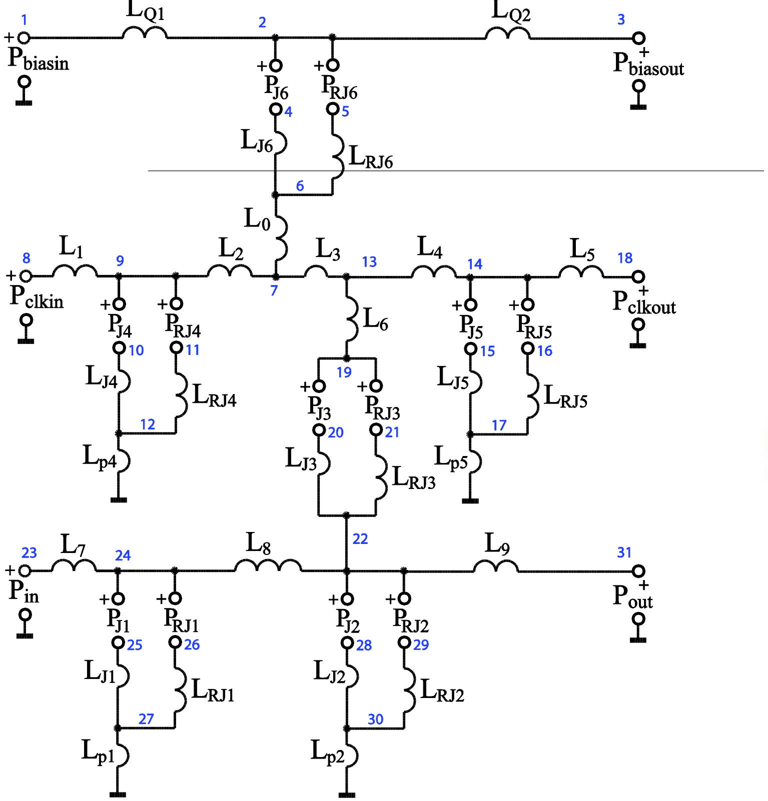
InductEx

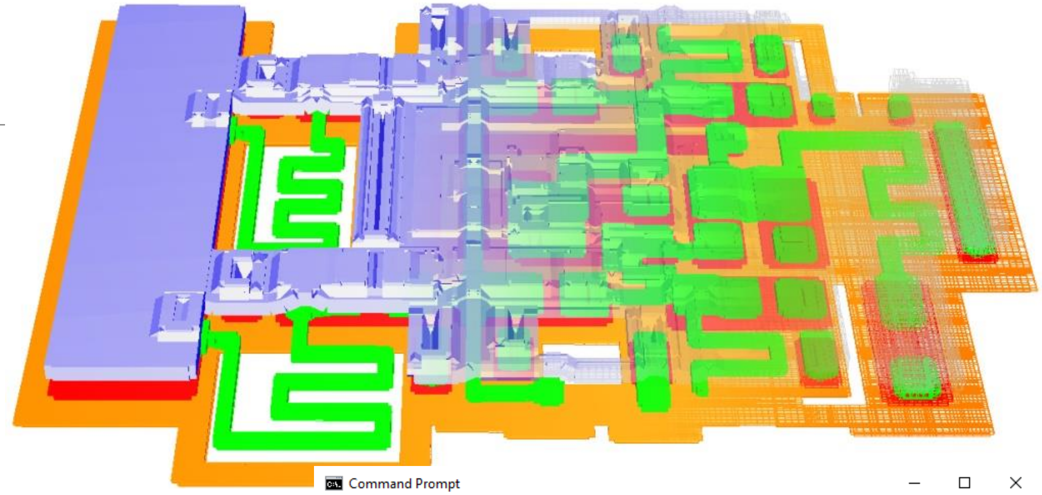
Developed to extract inductance from SC integrated circuits (works for semiconductors too).

- Console application (hooks into expensive EDA tools).
- Win, Linux, Mac.



InductEx





$$
\begin{array}{ccc} \mathbf{b} & \mathbf{A} & \mathbf{x} \end{array}
$$

$$
\begin{bmatrix} b_{P11} \\ b_{P12} \\ b_{P13} \\ b_{P21} \\ \vdots \\ b_{P33} \end{bmatrix} = \begin{bmatrix} 1+j0 \\ 1+j0 \\ 0 \\ -1+j0 \\ \vdots \\ -1+j0 \end{bmatrix} = \begin{bmatrix} I_{L1P1} & -I_{L2P1} & 0 & (I_{L2P1}-I_{L1P1}) \\ I_{L1P1} & 0 & -I_{L3P1} & I_{L2P1} \\ 0 & I_{L2P1} & -I_{L3P1} & I_{L1P1} \\ I_{L1P2} & -I_{L2P2} & 0 & (I_{L2P2}-I_{L1P2}) \\ \vdots & \vdots & \vdots & \vdots \\ 0 & I_{L2P3} & -I_{L3P3} & I_{L1P3} \end{bmatrix} \begin{bmatrix} Z_{L1} \\ Z_{L2} \\ Z_{L3} \\ j\omega M_1 \end{bmatrix}
$$

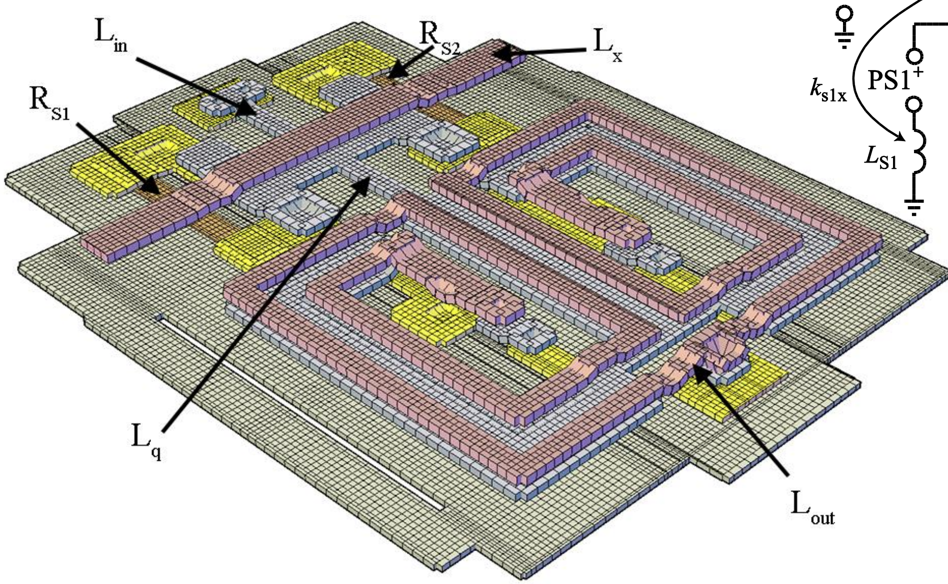
Command Prompt

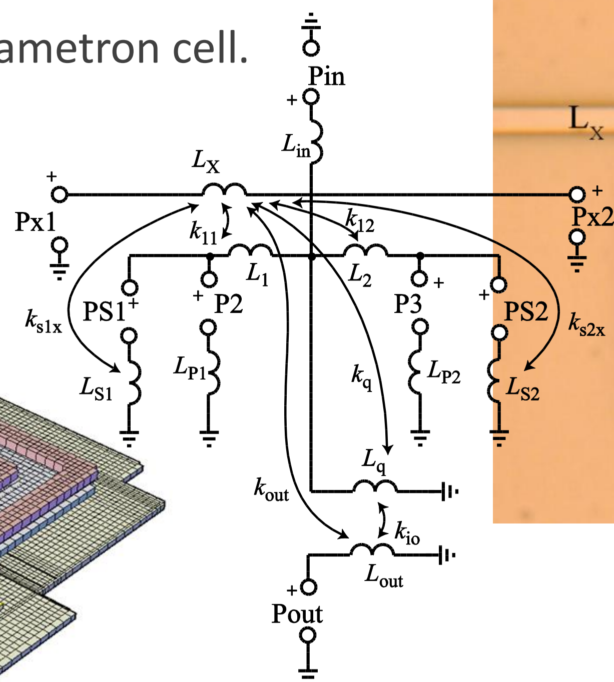
```
Reading ix.cur
Calculating SVD.

SVD info: Condition nr. = 8.28; unknowns = 62; rank = 62.

Impedance  Inductance [pH]       Resistance [Ohm]    AbsDiff    PercDiff
Name       Design    Extracted Design    Extracted (L only)  (L only)
L1         1.41500   1.27352   --        --        -0.1414   -10.00%
L2         0.44800   0.33395   --        --        -0.1140   -25.46%
L3         0.65900   0.65894   --        --        -0.0000   -0.01%
L4A        1.02000   0.91275   --        --        -0.1072   -10.51%
L4B        0.10000   0.12555   --        --        +0.0255   +25.55%
L5A        1.00000   0.83092   --        --        -0.1690   -16.91%
L5B        0.12200   0.38107   --        --        +0.2590   +212.35%
L6         1.48900   1.23973   --        --        -0.2492   -16.74%
L7         0.86200   0.59995   --        --        -0.2620   -30.40%
L8A        0.10000   0.04180   --        --        -0.0582   -58.20%
L8B        2.53400   2.58406   --        --        +0.0500   +1.98%
L15        0.82200   0.81575   --        --        -0.0062   -0.76%
L9         1.59000   1.61221   --        --        +0.0222   +1.40%
L10        0.55400   0.74165   --        --        +0.1876   +33.87%
L12        0.23100   0.15663   --        --        -0.0743   -32.19%
L16        1.27000   1.23314   --        --        -0.0368   -2.90%
L19        0.86900   0.60881   --        --        -0.2601   -29.94%
L13A       0.95100   1.06661   --        --        +0.1156   +12.16%
L13B       4.00000   3.28104   --        --        -0.7189   -17.97%
L18        1.73800   1.49203   --        --        -0.2459   -14.15%
L17        1.08400   0.70109   --        --        -0.3829   -35.32%
LP1        0.18600   0.11205   --        --        -0.0739   -39.76%
LP2        0.62500   0.69249   --        --        +0.0674   +10.80%
LP3        0.54500   0.62204   --        --        +0.0770   +14.14%
LP4        0.22100   0.10251   --        --        -0.1184   -53.61%
LIB1       1.00000   1.52223   --        --        +0.5222   +52.22%
LIB2       1.00000   0.40347   --        --        -0.5965   -59.65%
LIB3       1.00000   2.39137   --        --        +1.3914   +139.14%
LIB4       1.00000   0.56909   --        --        -0.4309   -43.09%
LIB5       1.00000   0.79409   --        --        -0.2059   -20.59%
LTUNE      1.00000   0.99502   --        --        -0.0049   -0.50%
Deallocating memory.
Cycles found in 0.257 seconds.
SVD solution in 0.408 seconds.
Job finished in 37.928 seconds.
```

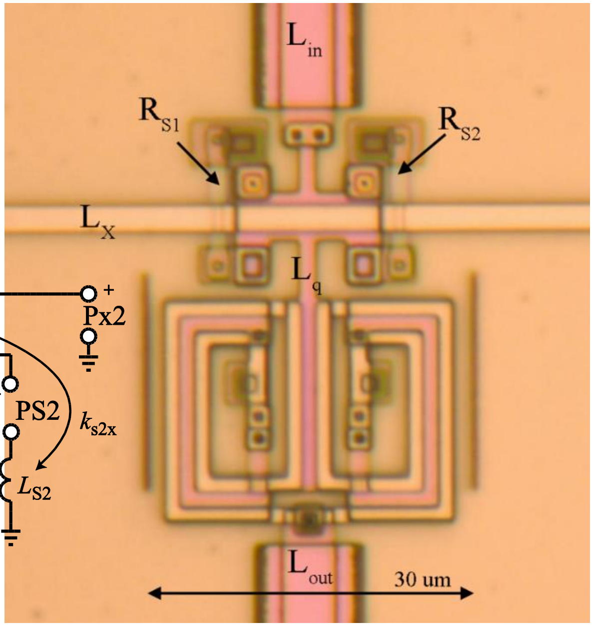
InductEx

Extraction of intentional and parasitic magnetic coupling.

This example: Quantum flux parametron cell.







InductEx

Developed in research time – no outside investment.

Commercialised through spin-off SUN Magnetics in 2015 as company's first (and premium) product.

Revenue model adopted:

- Price software in relation to value to customer.
- Use "lease" pricing – same licence fee every year to make customer retention as valuable as finding new customers.

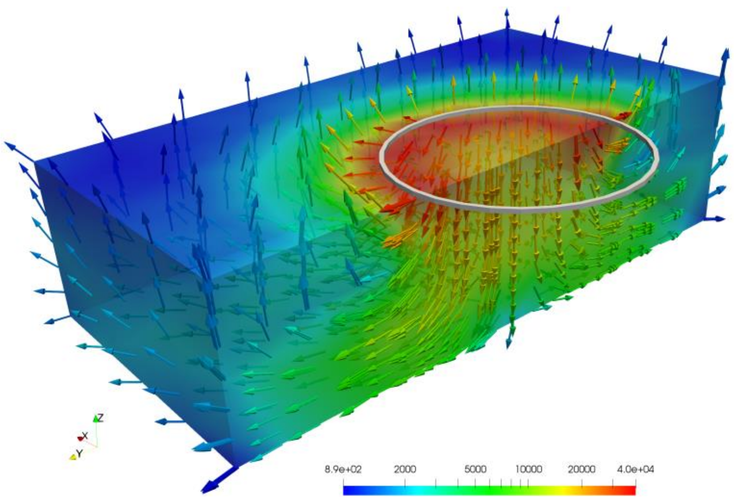
Added engineers from PhD cohort as revenue grew.

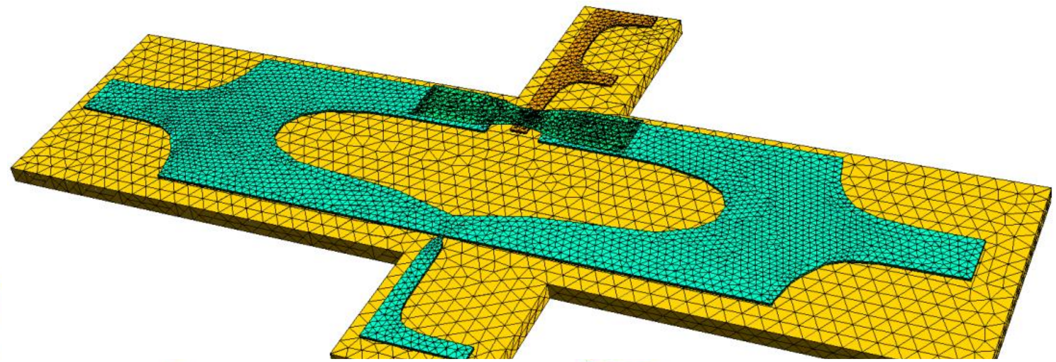
Dominant market capture in SCE/quantum.

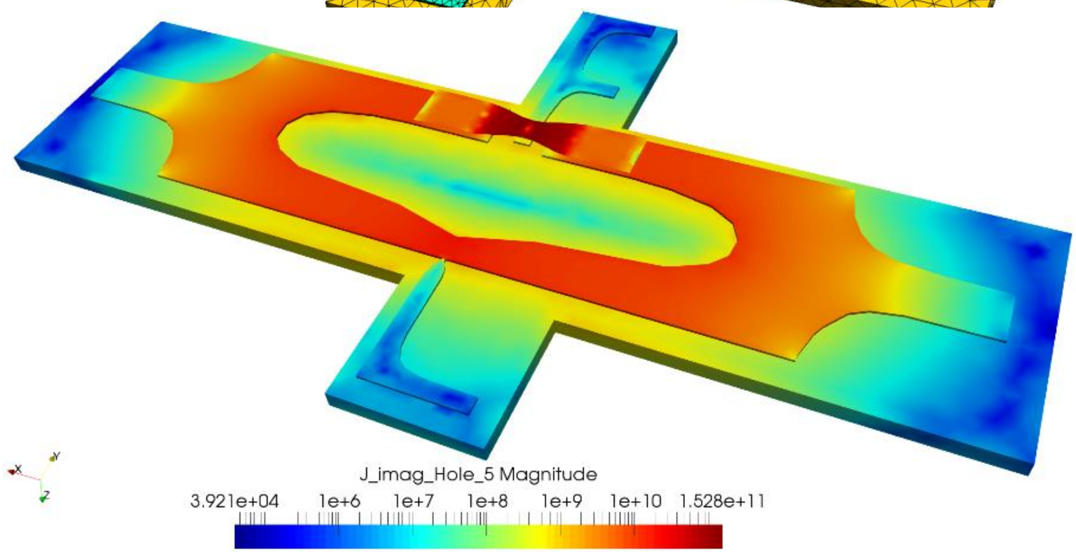
- Drawback of self-funding: slow growth.

InductEx: expanded functionality

Magnetic materials.

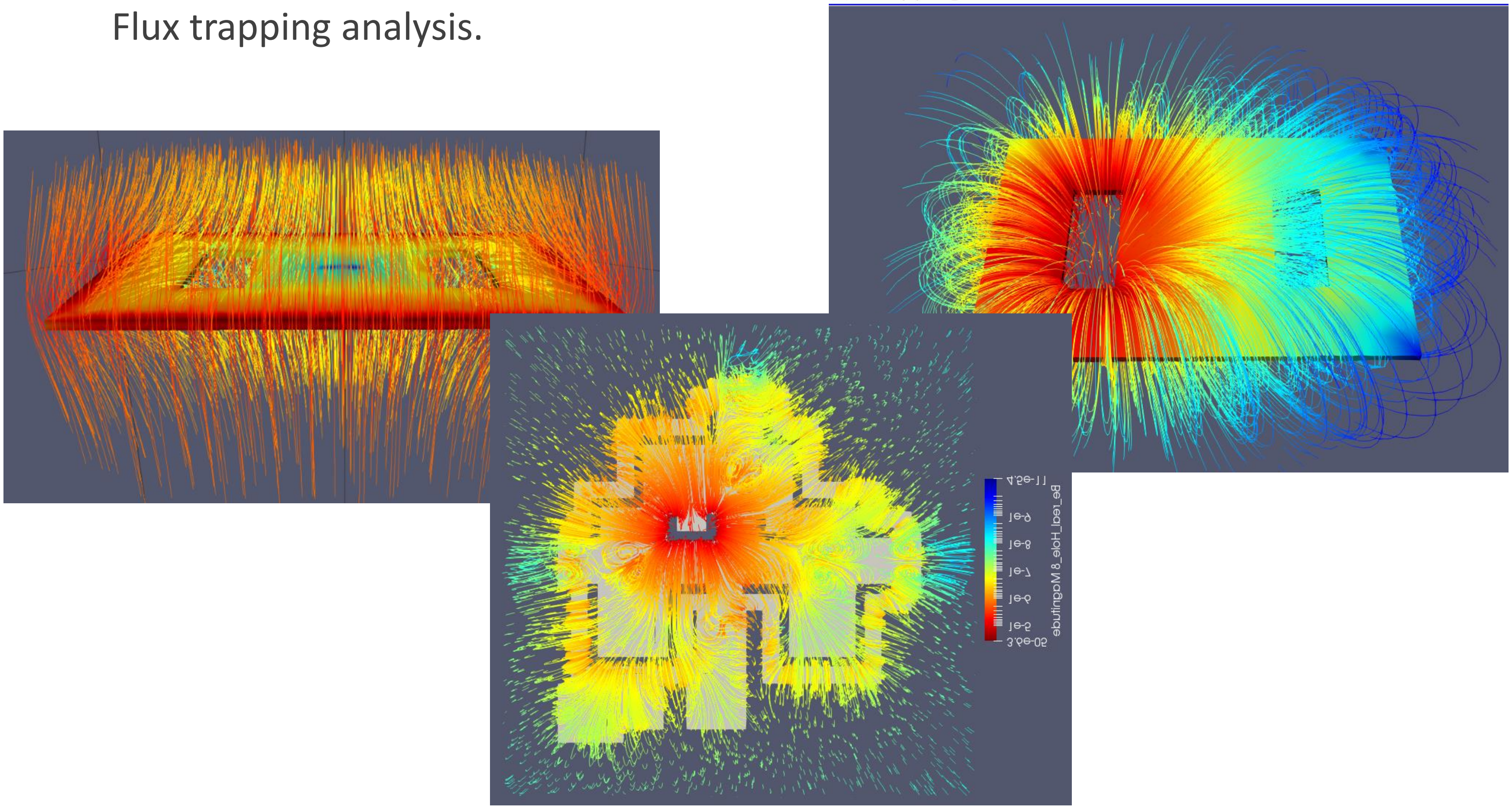






InductEx: expanded functionality

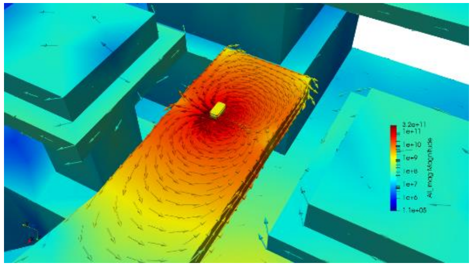
Flux trapping analysis.



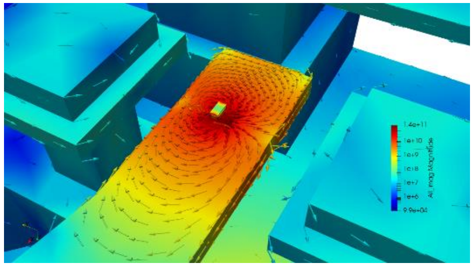
InductEx: expanded functionality

Spintronics:

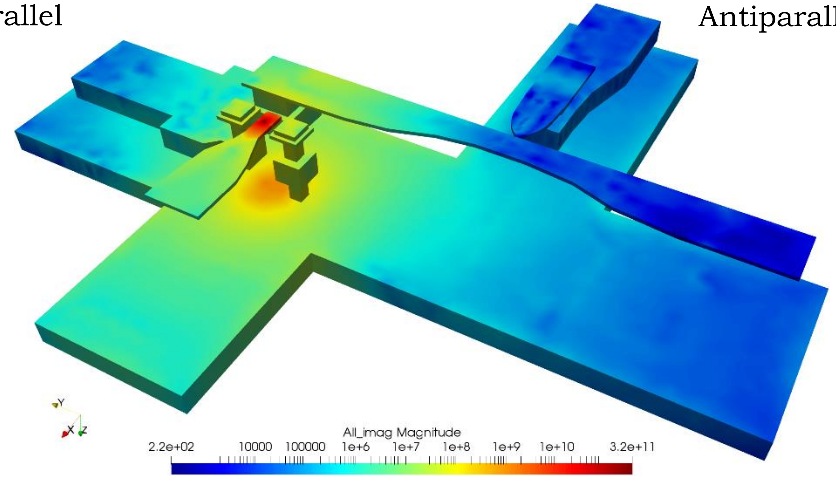
- Spin-Hall Effect devices with magnetized structures.



Parallel



Antiparallel



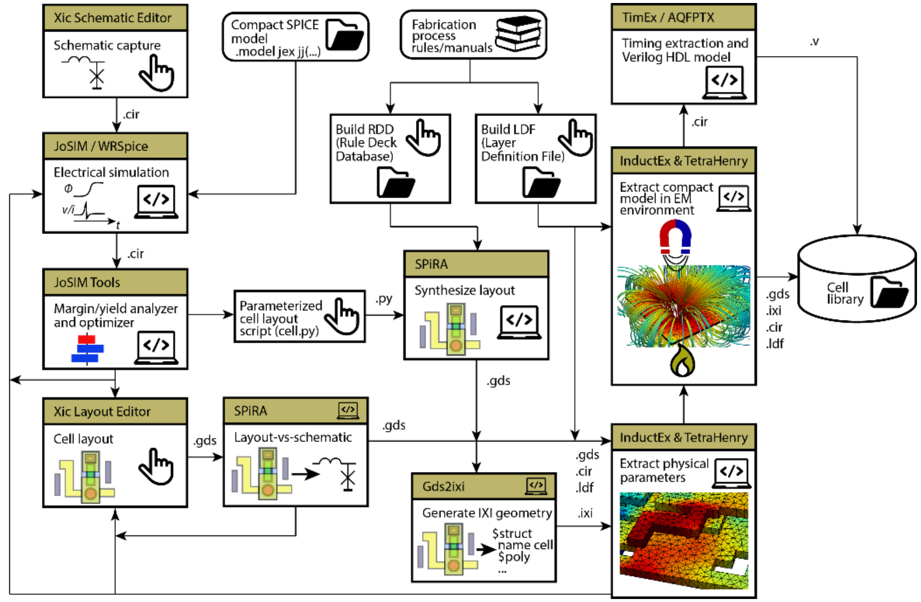
CSHE-nTron with current induced by magnetic pillar (log scale).

SUN Magnetics

InductEx extensively used in USA, Japan, China and France.

- Today, SCE chip design is considered almost impossible without it.
- Biggest customers: big companies in quantum computing.

With students, young engineers and innovation, expanded product range.



End notes

Human capacity development:

- Academic projects tied to start-ups retains young talent – leads to PhD (~2 per year from my group).

Retention in technological field (my students)

- Quantum electronic computer design/development.
- Design software for quantum electronics.
- Capacitive sensor IC development.
- Services (Takealot, Amazon).

Thank you